REMARKS/ARGUMENTS

Claims 1-8 and 12-23 are pending in the present application. Claims 1-5, 12-16 and 18-22 were amended and claims 9-11 were canceled to expedite prosecution. No claims were added. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. Double Patenting

The Examiner has provisionally rejected claims 1-3, 6-7, 9, 12-14, 17-20 and 23 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3-6, 8, 11, 13-15, 18 and 20-22 of copending Application No. 10/806,871.

In order to expedite prosecution, a Terminal Disclaimer is filed herewith to overcome the rejection. Therefore, the provisional rejection of claims 1-3, 6-7, 9, 12-14, 17-20 and 23 on the ground of nonstatutory obviousness-type double patenting has been overcome.

II. 35 U.S.C. § 101

The Examiner has rejected claims 18-23 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. This rejection is respectfully traversed.

The Examiner states:

> Claims 18-23 are not limited to tangible embodiments. In view of Applicant's disclosure, pg. 59, paragraph 1, the computer readable medium is not limited to tangible embodiments, instead being define as including both tangible embodiments (e.g. recordable-type media, such as a floppy disk, hard disk drive, a RAM, CD-ROMs, and DVD-ROMS) and intangible embodiments (e.g. transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions). As such, claims 18-23 are not limited to statutory subject matter and are therefore non-statutory.

Office Action dated October 5, 2006 at page 11.

Applicants respectfully disagree that claims 18-23 are directed to non-statutory subject matter. However, in order to expedite prosecution, claim 18 has been amended to recite a "recordable-type computer readable medium".

Therefore, the rejection of claims 18-23 under 35 U.S.C. § 101 has been overcome.

III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 4-12, 15-18 and 21-23 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,782,454 B1 to Damron (hereinafter "Damron"). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> 11. **As per claims 1 and 18**, Damron discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the method comprising:
>
> responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction (col. 4, lines 58-61; col. 5, lines 17-22; Fig. 1, element 175; Fig. 3, element 220); *It should be noted that computer program product in claims 18-23 executes the exact same functions as the methods in claims 1-6. Therefore, any references that teach claims 1-6 also teach the corresponding claims 18-23. It should also be noted that the "prefetch request" is analogous to the " instruction", the "prefetch engine" is analogous to the "processing unit", and the "starting address of a node, an offset value, and a termination value" all are analogous to the "metadata."*
>
> and responsive to metadata being present for the instruction, selectively prefetching data, from within a data structure using the metadata, into the cache in a processor (col. 5, lines 24-26; Fig. 3, element 225).

Office Action dated October 5, 2006 at page 12.

Claim 1 as amended herein is as follows:

> 1. A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:
>
> responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction;
>
> responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched; and
>
> responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Damron does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Damron does not teach or suggest "responsive to loading of an

instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction", and "responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched". In addition, Damron does not teach or suggest "responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor."

The Examiner refers to col. 4, lines 58-61 and col. 5, lines 17-22 of Damron as disclosing "responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction". These portions of Damron are reproduced below for the convenience of the Examiner:

> In accordance with the present invention, the data processing system **100** also includes a prefetch engine **175**. In one embodiment, prefetch engine **175** is an integrated circuit having a processor and an associated memory (not shown) configured to receive a prefetch request from processor **110**, prefetch data **150** in a node **145**, determine from the data an offset value and calculate from the offset value and the address of the first node **145A** the address for a second node **145B** to be prefetched.

Damron, col. 4, lines 57-65.

> In the method, a prefetch request from processor **110** is received in prefetch engine **175** (step **220**), and the data in the node prefetched. (step **225**) The prefetch request includes a starting address of a node, an offset value and a termination value.

Damron, col. 5, lines 17-22.

The above recitations describe only that a prefetch request is received in a prefetch engine and that the data in a node is prefetched. There is no teaching in the above recitations or elsewhere in Damron of determining, "responsive to loading of an instruction in the code into a cache", whether metadata for a prefetch is present for the instruction, or of determining "responsive to a determination of metadata being present for the instruction, whether data is to be prefetched". Damron simply performs a prefetch when a request is received. Damron does not make a determination whether metadata for a prefetch is present for an instruction and certainly does not disclose or suggest making a determination whether data is to be prefetched responsive to a determination of metadata being present for the instruction.

Damron also does not disclose or suggest "responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor" as recited in claim 1. Column 5, lines 24-26 of Damron referred to by the Examiner states only that "Generally, the step of prefetching data in the node, (step **225**), involves the step of writing data from node **145** to cache **160**." This is not a disclosure of prefetching data "responsive to a determination that data is to be prefetched" since, as indicated above, Damron never makes such a determination.

For at least all the above reasons, claim 1 is not anticipated by Damron and patentably distinguishes thereover in its present form.

Claims 4-8 depend from and further restrict claim 1 and are also not anticipated by Damron, at least by virtue of their dependency.

Independent claims 12 and 18 have been amended in a similar manner as claim 1, and are also not anticipated by Damron for similar reasons as discussed above with respect to claim 1. Claims 16-17 and 21-23 depend from and further restrict one of claims 12 and 18 and are also not anticipated by Damron, at least by virtue of their dependency.

Therefore, the rejection of claims 1, 4-12, 15-18, and 21-23 under 35 U.S.C. § 102(e) has been overcome.

Furthermore, Damron does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Damron actually teaches away from the presently claimed invention because it teaches prefeching data when a prefetch request is received in a prefetch engine as opposed to "responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction", "responsive to a determination of metadata being present for the instruction, determining whether data is to be prefetched", and "responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor" as in the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to implement Damron to include the steps recited in amended claim 1, one of ordinary skill in the art would not be led to modify Damron to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Damron in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

IV. 35 U.S.C. § 103, Obviousness (claims 2, 13 and 19)

The Examiner has rejected claims 2, 13 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Damron in view of IBM Technical Disclosure, Cache Miss Director – A Means of Prefetching Cache Missed Lines, August 1982, Vol. 25, Issue 3A (hereinafter "IBMTD"). This rejection is respectfully traversed.

Amended claim 2, which is representative of amended claims 13 and 19, is as follows:

> 2. The method of claim 1, wherein determining whether data is to be prefetched comprises: determining whether a number of outstanding cache misses is less than a threshold; and wherein the prefetching step comprises:

prefetching the data when it is determined that the number of outstanding cache misses is less than the threshold.

Claims 2, 13 and 19 depend from and further restrict one of claims 1, 12 and 18. IBMTD does not supply the deficiencies in Damron as described above. Claims 2, 13 and 19, accordingly, are patentable over the references, at least by virtue of their dependency. In addition, in rejecting the claims, the Examiner appears to acknowledge that Damron does not disclose the subject matter originally recited in claim 2, but contends that IBMTD discloses determining whether outstanding cache misses are present and "prefetching the data if a number of outstanding cache misses are less than a threshold". The Examiner further states that the phrase in original claim 2 of "if a number of outstanding cache misses are less than a threshold" has not been given any patentable weight because the term "if" denotes an optionally recited limitation not guaranteed to take place.

Applicants respectfully disagree with the Examiner's assertion that original claims 2, 13 and 19 contained language that suggests or makes optional, but does not require, steps to be performed or does not limit the claims to a particular structure. In order to expedite prosecution, however, claim 2 has been amended to recite "determining whether a number of outstanding cache misses is less than a threshold; and wherein the prefetching step comprises: prefetching the data when it is determined that the number of outstanding cache misses is less than the threshold", and claims 13 and 19 have been amended in a similar manner. These are positively recited limitations that cannot be simply ignored in rejecting the claims. IBMTD does not disclose these limitations, and claims 2, 13 and 19 patentably distinguish over the cited art in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 2, 13, and 19 under 35 U.S.C. § 103(a) has been overcome.

V. 35 U.S.C. § 103, Obviousness (claims 3, 14 and 20)

The Examiner has rejected claims 3, 14 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Damron in view of U.S. Patent No. 6,687,794 B2 to Malik (hereinafter "Malik"). This rejection is respectfully traversed.

Claim 3 as amended herein is as follows:

3. The method of claim 1, wherein determining whether data is to be prefetched comprises:
determining whether a number of cache lines chosen to be replaced is greater than a threshold; and wherein the prefetching step comprises:
prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the threshold.

Claims 3, 14 and 20 depend from and further restrict one of claims 1, 12 and 18. Malik does not supply the deficiencies in Damron as described above. Claims 3, 14 and 20, accordingly, are patentable over the references, at least by virtue of their dependency.

In addition, in rejecting the claims, the Examiner appears to acknowledge that Damron does not disclose the subject matter originally recited in claims 3, 14 and 20, but contends that Malik discloses determining whether to replace cache lines and "prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold". The Examiner states that the phrase in original claim 3 of "if a number of cache lines chosen to be replaced are greater than a threshold" has not been given any patentable weight because the term "if" denotes an optionally recited limitation not guaranteed to take place.

Applicants respectfully disagree with the Examiner's assertion that original claims 3, 14 and 20 contained language that suggests or makes optional, but does not require, steps to be performed or does not limit the claim to a particular structure, however, to expedite prosecution, claim 3 has been amended to recite "determining whether a number of cache lines chosen to be replaced is greater than a threshold; and wherein the prefetching step comprises: prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the threshold.", and claims 14 and 20 have been amended in a similar manner. These are positively recited limitations that cannot be simply ignored in rejecting the claims. Malik does not disclose these limitations, and claims 3, 14 and 20 patentably distinguish over the cited art in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 3, 14, and 20 under 35 U.S.C. § 103(a) has been overcome.

VI. Conclusion

For at least all the above reasons, claims 1-8 and 12-23 patentably distinguish over the cited art and are allowable in their present form. This application is, accordingly, believed to be in condition for allowance, and it is respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 5, 2007

Respectfully submitted,

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